Revision History

Rev. No.	History	Issue Date
2.0	Initial issue with new naming rule	Feb.15, 2005
2.1	Add 48CSP-6x8mm package outline	Mar. 08, 2005
2.2	Revise 48CSP-8x10mm pkg code from W to K	Oct. 25, 2005
2.3	Revised DC characteristics	Nov. 23, 2006
2.4	Revised DC characteristics	Jun. 20,2007
2.5	Change wafer process from 0.18um to 0.15um	May. 19, 2008
2.6	Add CE2 description of 48BGA package	Nov. 20, 2009
2.7	Modify Data Retention waveform	May. 27.2010

■ PRODUCT DESCRIPTION

The CS16LV81923 is a high performance, high speed, low power CMOS Static Random Access Memory organized as 524,288 words by 16 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced 0.15um CMOS technology and circuit techniques provide both high speed and low power features with a Typical CMOS standby current of 0.3uA and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable1 (/CE), active HIGH chip enable2 (CE2) for BGA product and active LOW output enable (/OE) and three-state output drivers.

The CS16LV81923 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV81923 is available in JEDEC standard 44L TSOP 2 and 48Ball Mini_BGA 8x10mm packages.

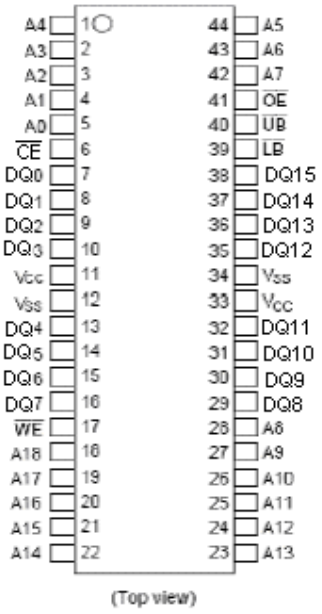
■ FEATURES

- Low operation voltage: 2.7 ~ 3.6V
- Ultra low power consumption:
  Vcc = 3.0V: 25mA (Typ.) operating current, 0.3uA (Typ.) CMOS standby current
- High speed access time: 55/70ns (Max.) at Vcc = 3.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE&CE2 and /OE options.

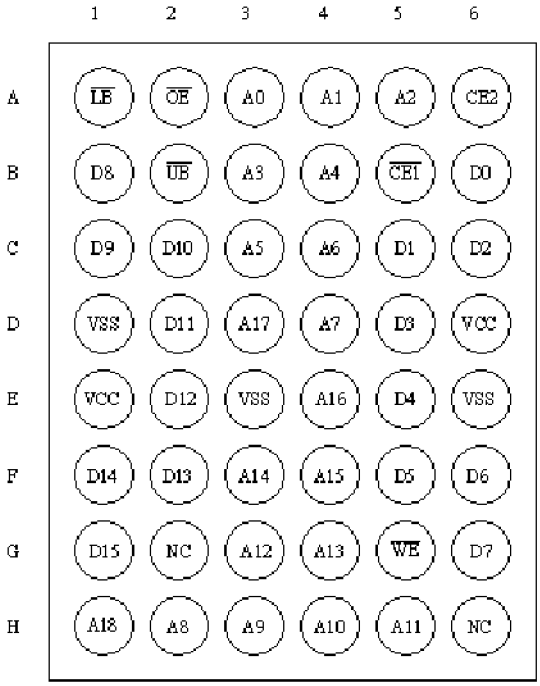
■ PRODUCT FAMILY

Product Family	Operating Temp	Vcc. Range	Speed (ns)	Standby Current (Typ.)	Package Type
CS16LV81923	0 ~ 70°C	2.7 ~ 3.6	55/70	0.3 uA (V_{CC} = 3.0V)	44 TSOP 2-400mil 48 Mini_BGA 8x10mm
	-40 ~ 85°C			0.3 uA (V_{CC}= 3.0V)	

■ PIN CONFIGURATIONS

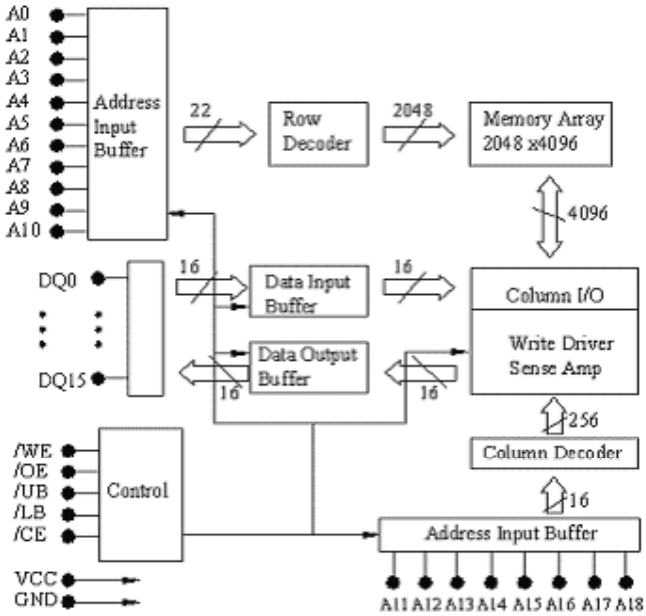


44-TSOP2 : Top view

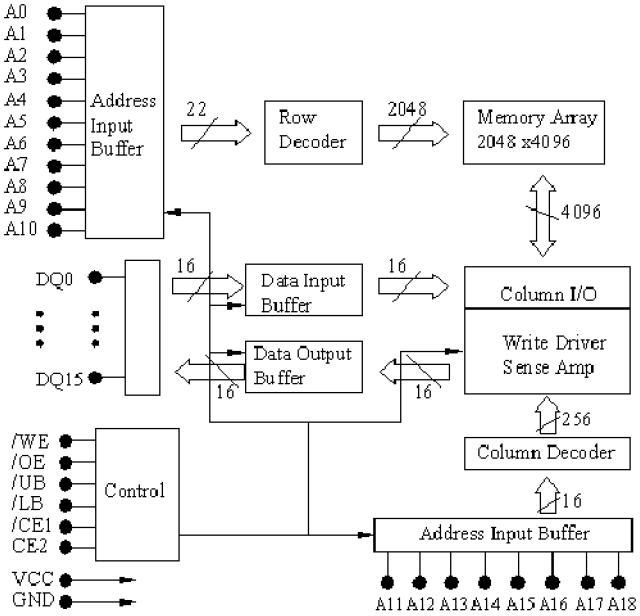


48 Ball CSP - Top View

■ FUNCTIONAL BLOCK DIAGRAM



For single CE product of 44 TSOP 2-400mil



For dual CE product of 48 Mini_BGA 8x10mm

■ PIN DESCRIPTIONS

Name	Type	Function
A0 ~ A18	Input	19 address inputs for selecting one of the 524,288 x 16 bit words in the RAM
/CE **/CE1 & CE2**	Input	/CE1 is active LOW and CE2 is active high. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power	Power Supply
Vss	Power	Ground

■ TRUTH TABLE

MODE	/CE(1)	/CE1(2)	CE2(2)	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	Vcc Current
Fully Standby	H	H	X	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	X	X	L	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	L	H	H	H	X	X	High Z	High Z	I_{CC}
Read	L	L	H	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
						H	L	High Z	D_{OUT}	I_{CC}
						L	H	D_{OUT}	High Z	I_{CC}
Write	L	L	H	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
						H	L	High Z	D_{IN}	I_{CC}
						L	H	D_{IN}	High-Z	I_{CC}

Note: (1) /CE is used for 44 TSOP 2-400mil of single CE product only.

(2) /CE1 and CE2 are used for 48 Mini_BGA 8x10mm dual CE product only.

■ ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.2 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	35	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ DC ELECTRICAL CHARACTERISTICS (TA = 0~+70°C / -40°C~+85°C ,V_{CC} = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)		-0.2(2)		0.6	V
V_{IH}	Guaranteed Input High Voltage (2)		2.2		Vcc+0.2(2)	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IH}, or /OE=V_{IH} , V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2 mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	2.4			V
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX}(3)		25	35	mA
I_{CCSB}	Standby Supply -TTL	/CE=V_{IH}, I_{DQ}=0mA,			0.5	mA
I_{CCSB1}	Standby Current-CMOS	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.3	6	uA

1. Typical characteristics are at TA = 25°C.
2. Overshoot: Vcc+2.0V in case of pulse width ≦20ns. Undershoot: -2.0V in case of pulse width ≦20ns. Overshoot and undershoot are sampled, not 100% tested.
3. Fmax = 1/t_{RC}.

■ OPERATING RANGE

Range	Ambient Temperature	V_{CC}
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

■ CAPACITANCE (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	8	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	10	pF

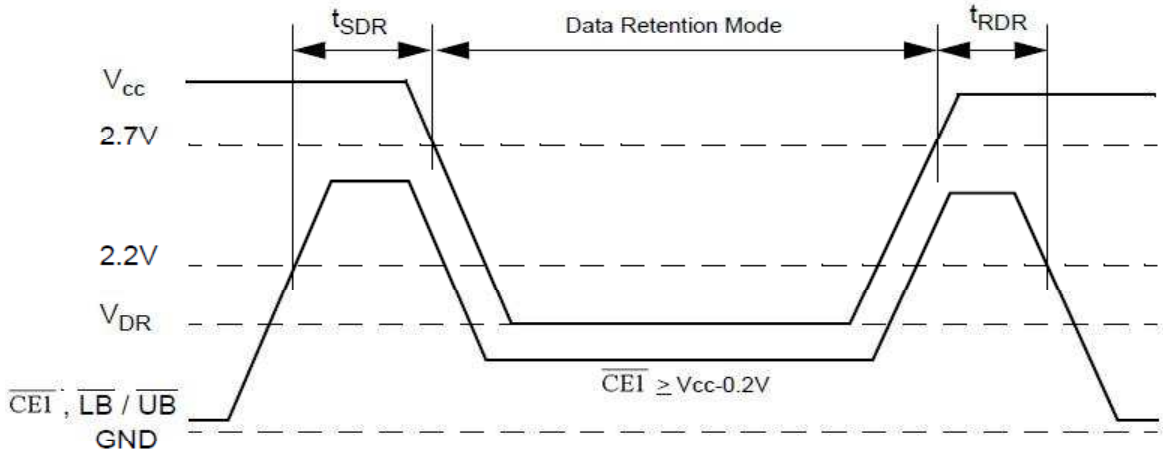
1. This parameter is guaranteed and not 100% tested.

■ DATA RETENTION CHARACTERISTICS (TA = 0~+70°C / -40°C~+85°C)

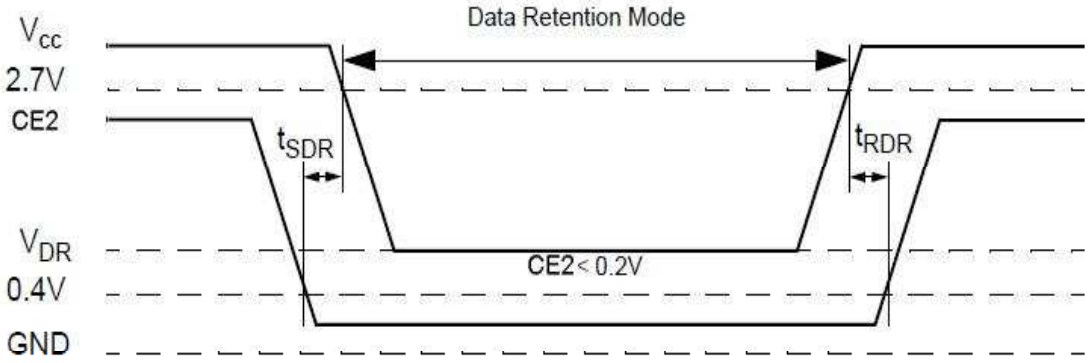
Parameter Name	Parameter	Test Conduction	MIN	TYP(1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{CC}=1.5V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.1	3	uA
t_{SDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_{RDR}	Operation Recovery Time		t_{RC} (2)			ns

1. V_{CC}= 3.0V, T_A = +25°C
2. t_{RC} (2)= Read Cycle Time.

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE1 or /CE Controlled)



■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled-BGA only)



■ KEY TO SWITCHING WAVEFORMS

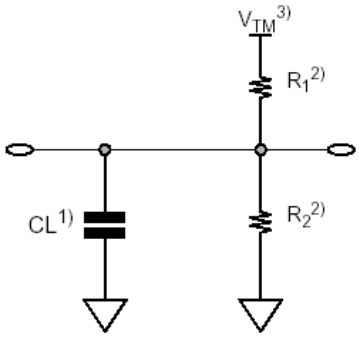
WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

■ AC TEST LOADS

Input Pulse Level : 0.4 to 2.4V
Input Rise and Fall Time : 5ns
Input and Output reference Voltage : 1.5V
Output Load (See right) : CL = 100pF+ 1 TTL

$CL^{1)}$ = 30pF + 1 TTL

1. Including scope and Jig capacitance
2. R_1=3070 ohm, R_2=3150 ohm
3. V_{TM}=2.8V



■ AC ELECTRICAL CHARACTERISTICS(TA = 0~+70°C / -40°C~+85°C , Vcc = 3.0V)

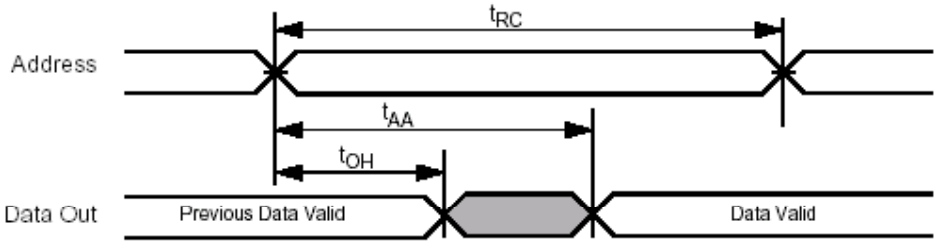
< READ CYCLE >

JEDEC Name	Parameter Name	Description	55		70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{CO}	Chip Select Access Time (/CE)		55		70	ns
t_{BA}	t_{BA}	Data Byte Control Access Time (/LB, /UB)		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		30		35	ns
t_{ELQX}	t_{LZ}	Chip Select to Output Low Z (/CE)	5		5		ns
t_{BE}	t_{BLZ}	Data Byte Control to Output Low Z (/LB, /UB)	10		10		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{HZ}	Chip Deselect to Output in High Z (/CE)	0	20	0	20	ns
t_{BDO}	t_{BHZ}	Data Byte Control to Output High Z (/LB, /UB)	0	20	0	20	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	0	20	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		ns

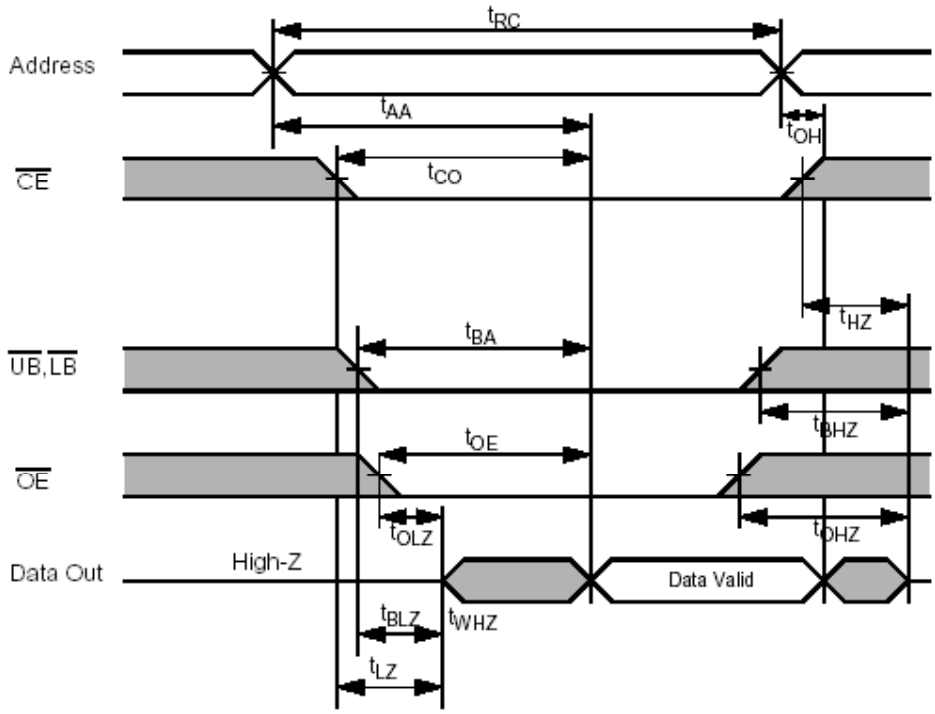
■ SWITCHING WAVEFORMS (READ CYCLE)

For single CE product of 44 TSOP 2- 400mil

TIMING WAVEFORM OF READ CYCLE(1). (Address Controlled. /CE=/OE=VIL, /UB or/and /LB=VIL)



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})

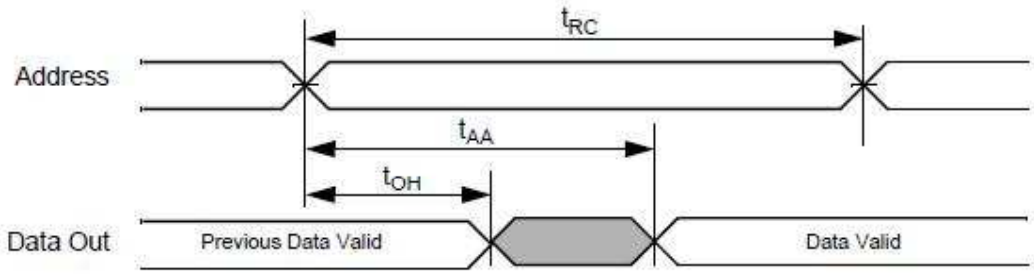


NOTES:

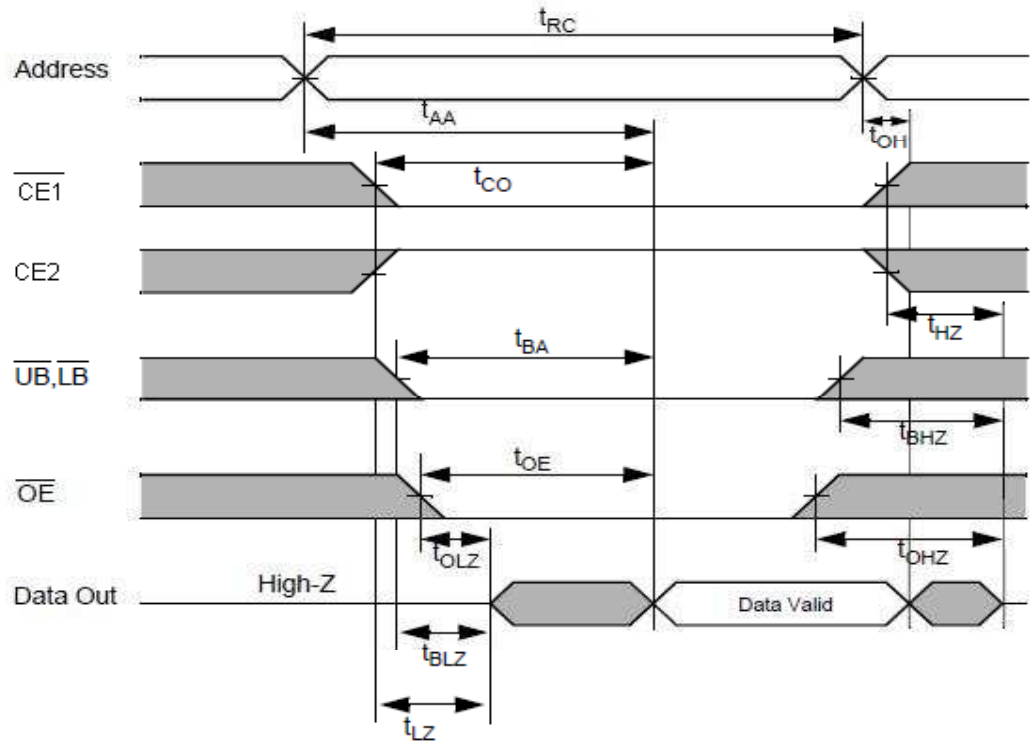
1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

For dual CE product of 48 Mini_BGA 8x10mm

TIMING WAVEFORM OF READ CYCLE(1). (Address Controlled, /CE1=/OE=VIL, CE2=/WE=VIH)



TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$ = V_{IH})



NOTES:

1. t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

■ AC ELECTRICAL CHARACTERISTICS (TA = 0~+70°C / -40°C~+85°C , Vcc = 3.0V)

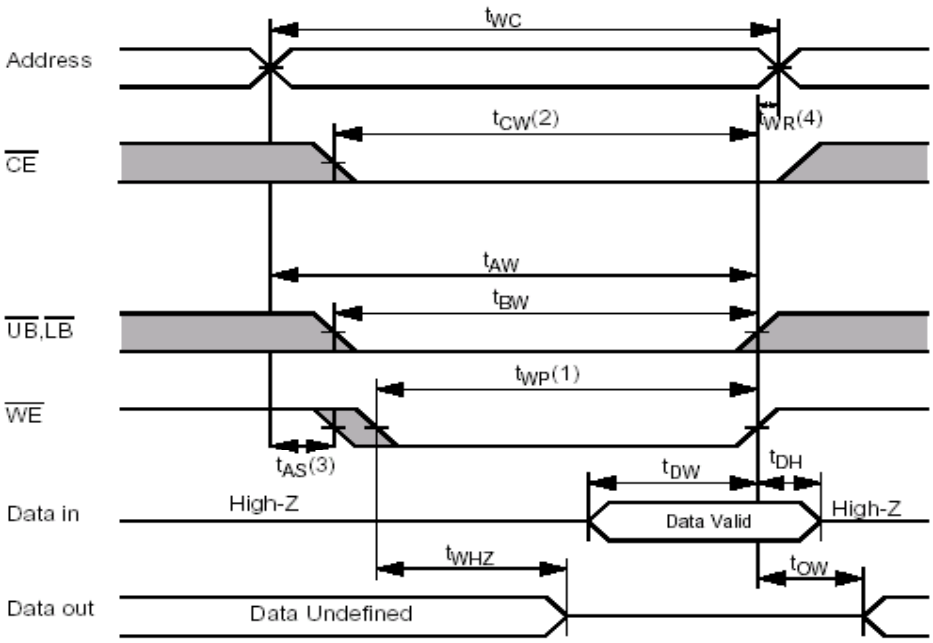
< WRITE CYCLE >

JEDEC Name	Parameter Name	Description	55		70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	45		55		ns
t_{WHAX}	t_{WR}	Write Recovery Time (/CE, /WE)	0		0		ns
t_{BW}	t_{BW}	Data Byte Control to End of Write(/LB, /UB)	55		70		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	20	0	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

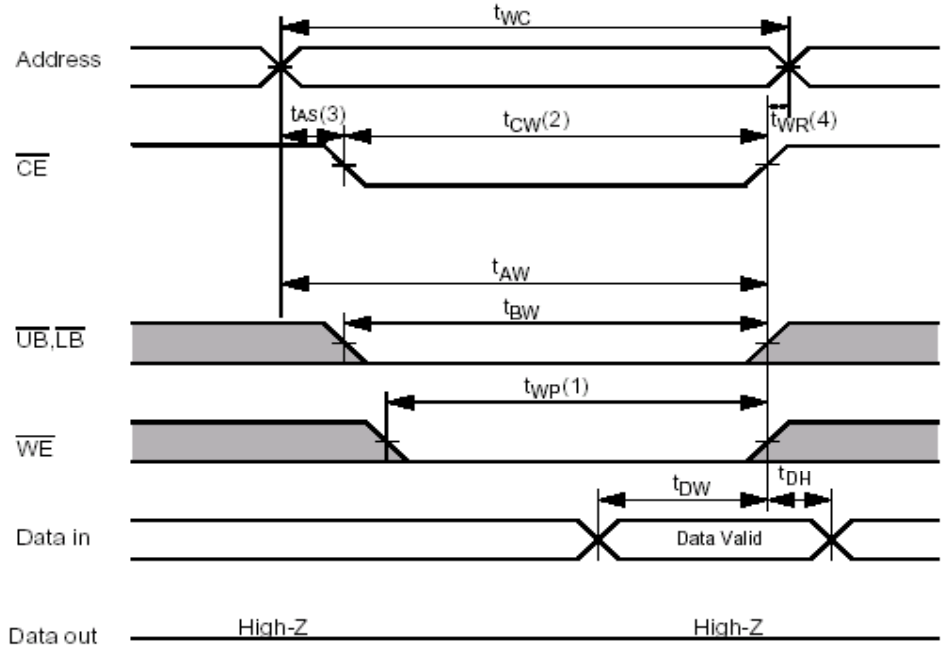
■ SWITCHING WAVEFORMS (WRITE CYCLE)

For single CE product of 44 TSOP 2- 400mil

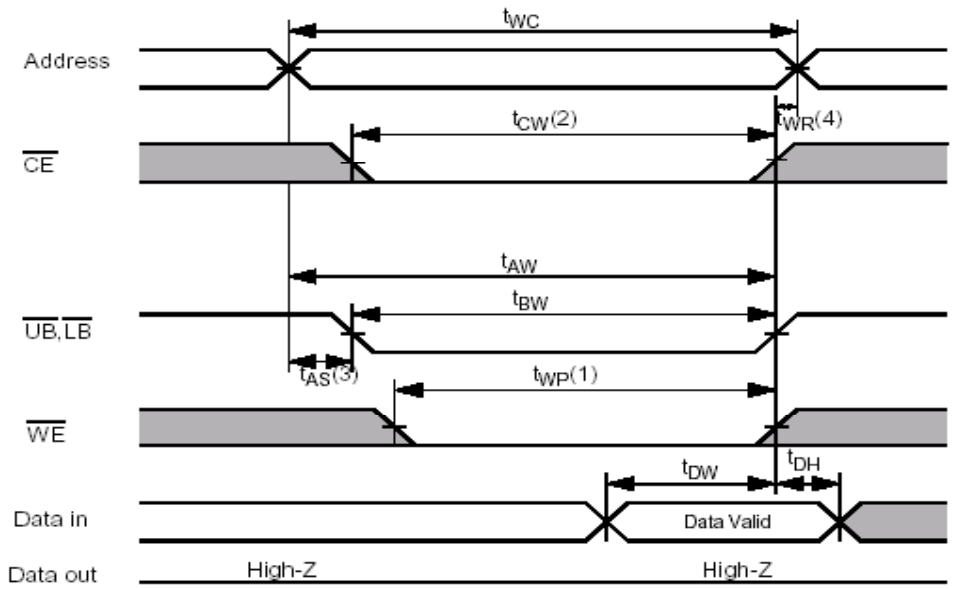
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ CONTROLLED)

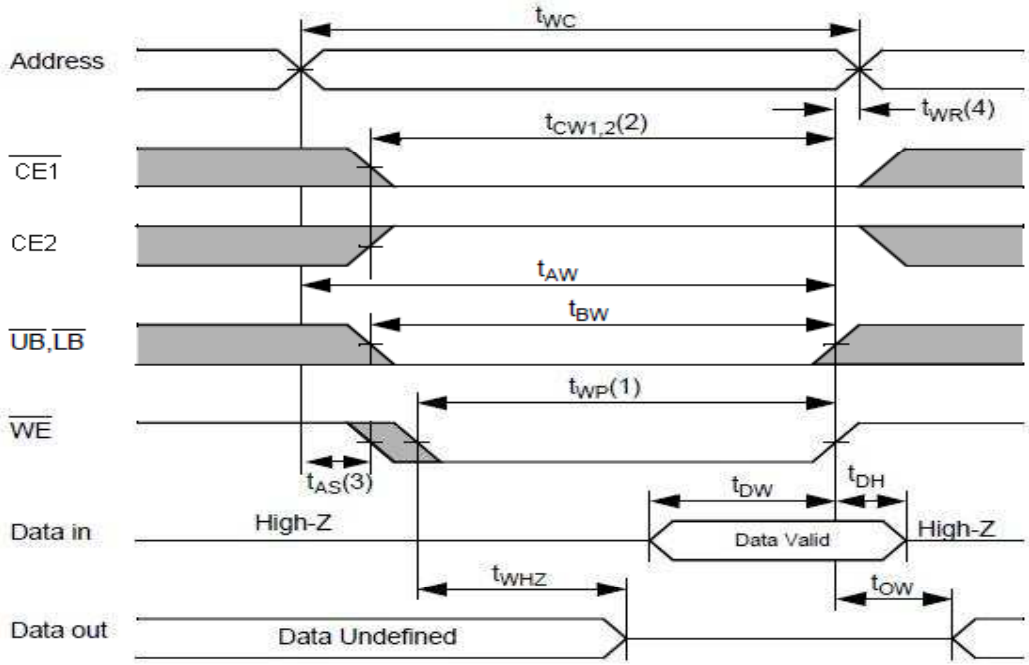


NOTES:

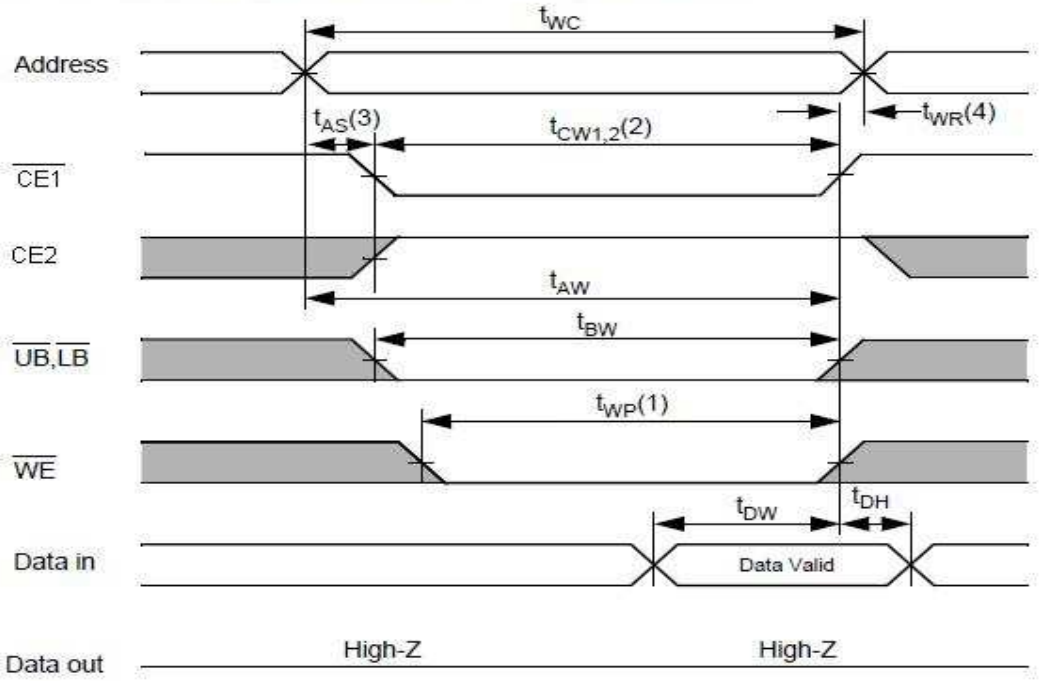
1. A write occurs during the overlap(t_{WP}) of low /CE and low /WE. A write begins when /CE goes low and /WE goes low with asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CE goes high and /WE goes high. The t_{WP} is measured from the beginning of the write to the end of write.
2. t_{CW} is measured from the /CE going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. T_{WR} applied in case a write ends as /CE or /WE going high.

For dual CE product of 48 Mini_BGA 8x10mm

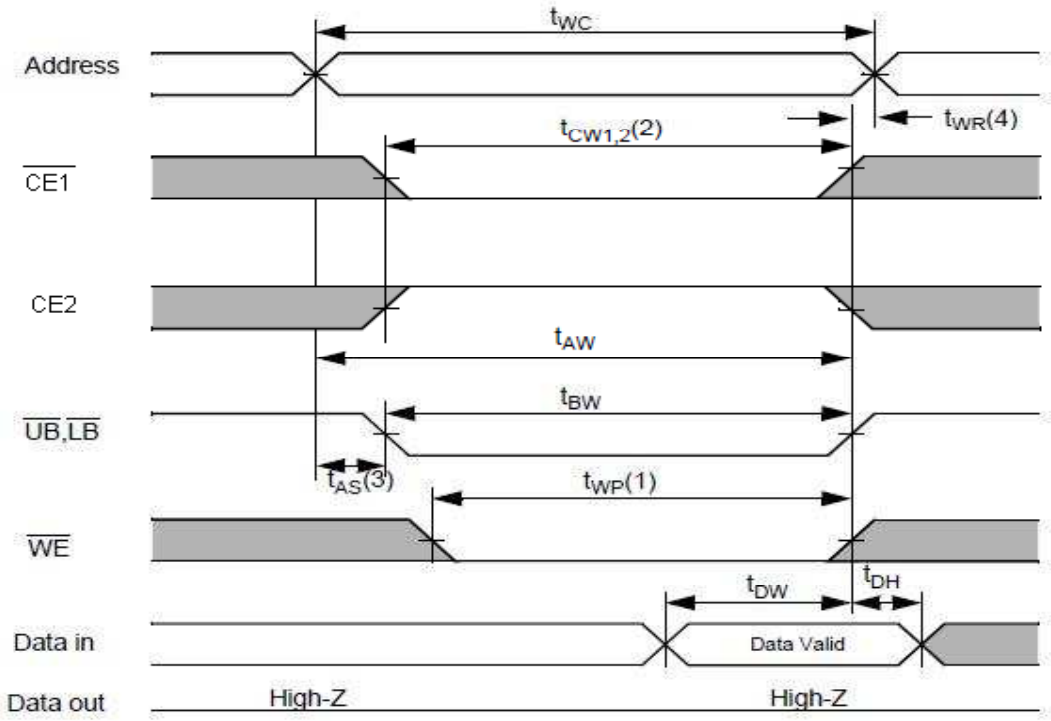
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ CONTROLLED)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CE1}$ CONTROLLED)



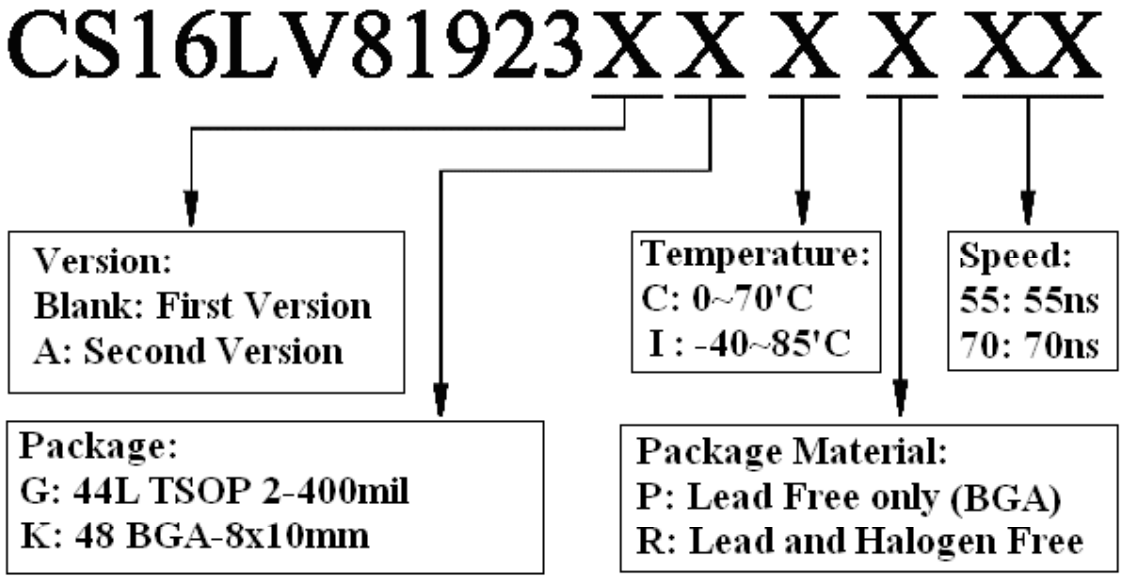
TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ CONTROLLED)



NOTES:

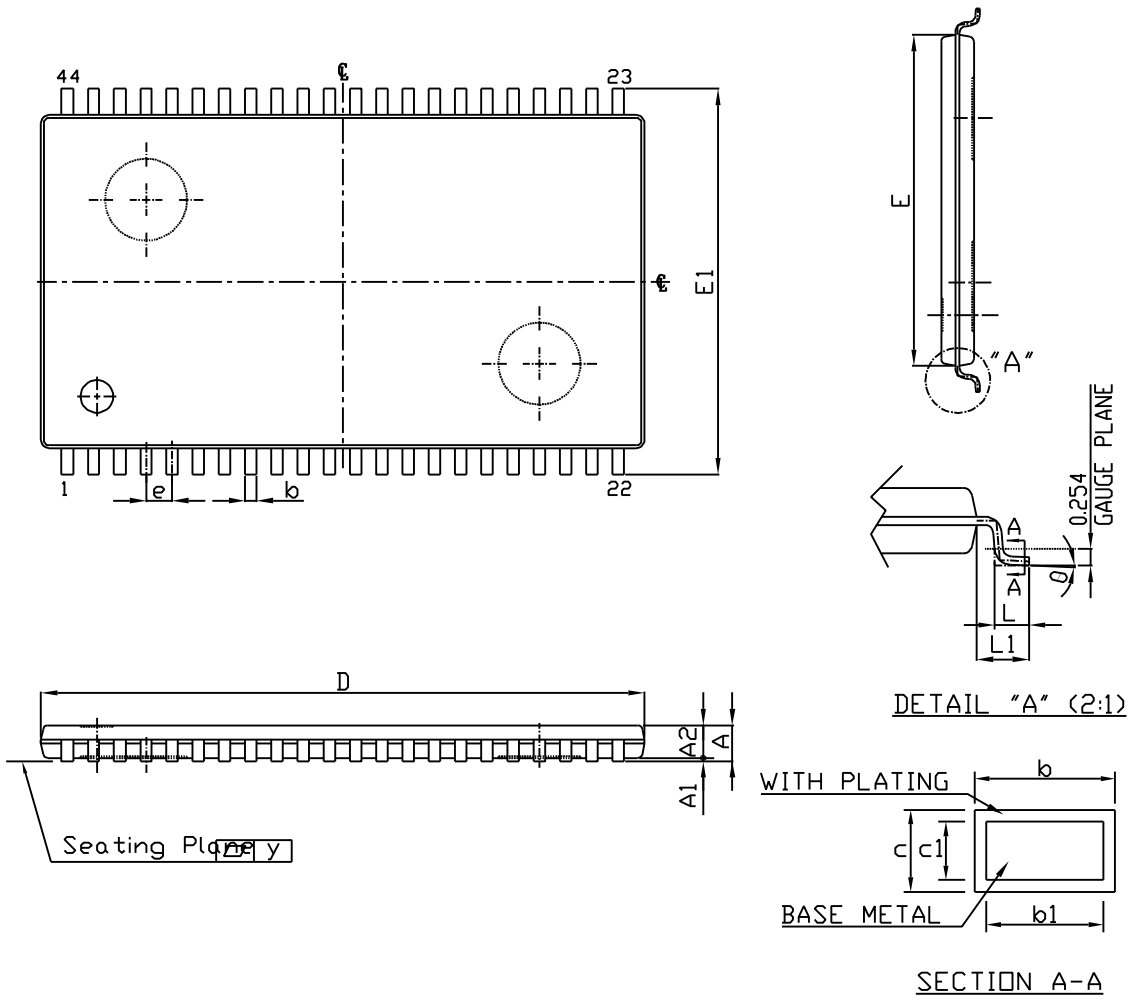
1. A write occurs during the overlap(t_{WP}) of low /CE1, high CE2and low /WE. A write begins when /CE1 goes low, CE2 goes high and /WE goes low with asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CE1 goes high, CE2 goes low and /WE goes high. The t_{WP} is measured from the beginning of the write to the end of write.
2. t_{CW} is measured from the /CE1 going low or CE2 going high to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. T_{WR} applied in case a write ends as /CE1 going high, CE2 going low or /WE going high.

■ ORDER INFORMATION



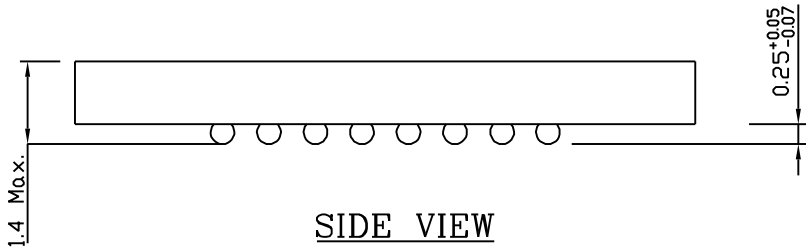
Note: Package material code “P” & “R” comply with RoHS.

■ PACKAGE DIMENSIONS: 44L TSOP 2-400mil



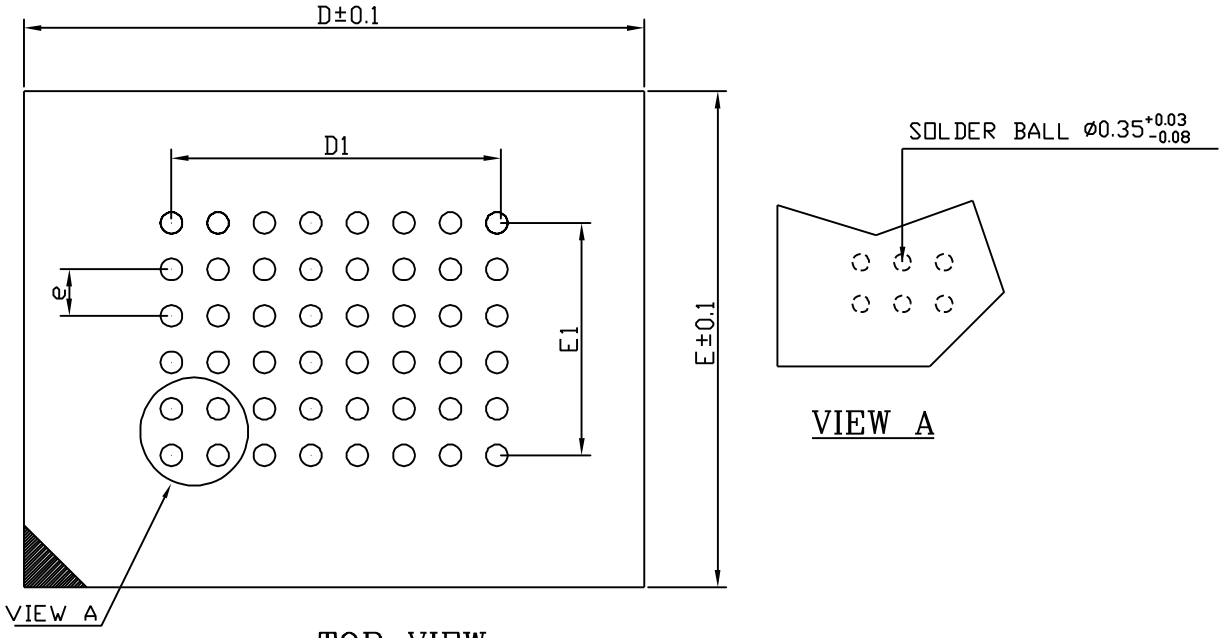
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	-	0°
	Nom.	1.10	0.10	1.00	-	-	-	-	18.41	10.16	11.76	0.80	0.50	0.80	-	-
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	-	-	-	-	0.725	0.400	0.463	0.0315	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

■ PACKAGE DIMENSIONS: 48 ball Mini_BGA-8x10mm



SIDE VIEW

BALL PITCH e = 0.75				
D	E	N	D1	E1
10.0	8.0	48	5.25	3.75



TOP VIEW

VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.